Notice of Allowability	Application No.	Applicant(s)	
	10/786,403	KOBAYAKAWA, MASAHIKO	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the election made on 6/20/05*.

2. ☒ The allowed claim(s) is/are *1-3 and 5-7*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/044,231* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Examiner's amendment

The elected claims 1-3,5-7 have been examined and the non-elected rest canceled because election was made without traverse.

Statement of reasons for allowance

Claims 1-3,5-7 have been have been allowed.

Semiconductors chips such as those in figure 3 of PN: 6,858,879 have been designed to be positioned on a first terminal electrode and the upper surface supplied with another terminal connected to a second terminal at the level of the first terminal by wiring means and the entire structure sealed and only exposing the first and second terminal surfaces (4 and 5). But such a structure is taught to raise problems on wiring (11) as specified in the specification of pages 5-6.

Another relevant art is figure 13C of PN: 6,897,096 whereby a chip (120h) is mounted and directly attached to a conductor underneath and the top terminals connected to terminals outside the mounting area but at the same level of the directly connected terminal. But such a structure is taught to raise problems on wiring (123) as specified in the specification of pages 5-6.

Another relevant art seems to be figure 2 of PN: 6,812,552.The structure in figure 2C shows that a chip can be mounted on and directly attached to more than one terminal while figure 2a shows that the upper surface of a chip can have terminals attached to terminals under the chip by wiring means (60). The structures, however, are bound to suffer from the same problems taught in the specification because the chip is

not positioned directly on the terminal/s specifically when the wiring (60) is applicable in the structure.

Figure 8 of PN: 6,664,621 shows a chip on terminals (301) separated by adhesive material (333) on a substrate and both terminals connected to upper terminals of the chip by wiring means (303). Clearly the structure does not show a third conductor partially supported by the upper surface of the chip as in the structure of the claimed invention. The art, however, partially reads on the claimed invention but lacks the additional features associated with direct contact between a lower terminal and said second conductor on the second surface of the chip and the sealant feature that seals the structure except the surfaces of said first and second conductors.

While the general concept of wiring problems in the prior art structures was discussed in relation to figures 43-46 of the specification and the connection between said first and second conductors in relation to the terminals on the chip surfaces individually have been known in the art, the claimed invention whereby first and second terminals of the same level are provided to mount a chip, the chip directly in contact with one of the terminals through a terminal on the second (lower) surface and with the other terminal by wiring means through a terminal on its first (upper) surface, the structure designed such that the weight of the chip lands on the two terminals through the second surface in order to resolve wiring stress specifically of the one that connects the upper chip terminal with one of the terminals under the chip as described in pages 5-7 of the specification is not taught or rendered obvious by the prior arts.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Refer to PN: 6,897,096: 6,812, 552, 6,664,621.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
9/11/05